PIC18F2331/2431/4331/4431 Rev. A3 Silicon Errata

The PIC18F2331/2431/4331/4431 parts you have received conform functionally to the Device Data Sheet (DS39616), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2331/2431/4331/4431 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All the issues listed here will be addressed in future revisions of the PIC18F2331/2431/4331/4431 silicon. **The following silicon errata apply only to PIC18F2331/2431/4331/4431 devices with these Device/Revision IDs**:

Part Number	Device ID	Revision ID
PIC18F2331	00 1000 111	00010
PIC18F2431	00 1000 110	00010
PIC18F4331	00 1000 101	00010
PIC18F4431	00 1000 100	00010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: PCPWM

When the PCPWM is operated in Complementary mode with a non-zero dead-time value and the duty cycle results in an active-low time of less than 1 TCY, the PWM generator will miss the rising edge for a new PWM period and the PWM output will alternate between one PWM period high and one PWM period low.

Work around

When in Complementary mode with a non-zero dead-time value, ensure that the active-low time will always be greater than 1 TCY. In other words, when dead time is not equal to zero, ensure that:

PDCH:PDCL < (4 * PTPERH:PTPERL)

or

PDCH:PDCL > (4 * (PTPERH:PTPERL + 1))

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: PCPWM

When the PCPWM is operated in Center-Aligned mode with double updates and the duty cycle alternates on each update between a zero and non-zero value, an incorrect waveform is generated (the PWM output will alternate between one PWM period high and one PWM period low). If in Complementary mode, dead time will not be inserted properly.

Work around

Do not use zero duty cycle when in Center-Aligned mode with double updates. Instead of zero, set the duty cycle to a small, non-zero value.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: PCPWM

When the PCPWM is operated in Center-Aligned mode with double updates and the duty cycle alternates on each update between a greater than 100% duty cycle and a non-zero value, an incorrect waveform is generated.

Work around

Do not use equal to or greater than 100% duty cycle when in Center-Aligned mode with double updates. Ensure that the maximum duty cycle value is always smaller than or equal to the PWM period, i.e., PDCH:PDCL ≤ (4 * (PTPERH:PTPERL)).

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: PCPWM

If dead-time insertion is enabled and it is a non-zero value, glitches in the PWM output will occur under the following conditions:

1. When the PWM timer is stopped by clearing the PTEN bit.
2. When the duty cycle is changed to zero.

Work around

1. Before disabling the PWM timer, ensure that PORTB is set up to maintain a safe state of external hardware and that TRISB is set up to define the pins as outputs.
2. Do not use zero duty cycle when dead-time insertion is enabled. Instead of zero, set the duty cycle to a small, non-zero value (such as '1').

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: PCPWM

The PTMRH register will read as '00' or the last value written to it, even though the upper four bits of the PWM timer may be different. Writing to PTMRH **will** effect the upper four bits of the PWM timer when PTMRL is subsequently written. Although the PWM timer operates correctly, the double-buffer circuit does not transfer data to the PTMRH register from the upper four bits of the PWM timer.

Work around

PWM operation is not affected. Do not attempt to read PTMRH.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: PCPWM

In Complementary mode with dead-time insertion, when using OVDCOND and OVDCONS to override the PWM outputs, dead time is not inserted correctly when the dead-time prescaler is FOSC/4, FOSC/8 or FOSC/16.

Work around

None. Use dead-time prescaler of FOSC/2 in these circumstances.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: Core (DAW Instruction)

The DAW instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the DAW instruction. If the Carry bit is set, increment the next higher byte to be added, using an instruction such as INCFSZ (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the DAW instruction has been executed, process the Carry bit normally (see Example 1).

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB

This is repeated for each DAW instruction.
```

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: EUSART

Bit SENDB in the TXSTA register is not automatically cleared by hardware upon completion of transmission of a Sync Break.

Work around

Check the TRMT bit in TXSTA. If the TRMT bit is set, Break transmission is said to be complete.

9. Module: EUSART

If the transmitter is left enabled while the module is performing an auto-baud operation, an arbitrary data byte may get transmitted.

Work around

Clear TXEN bit (TXSTA<5>) before any auto-baud operation and set it after auto-baud is complete. Enable TXEN only when a data byte is to be transmitted. Care must be taken to ensure that the TX pin is pulled high, either through an external resistor, or by making the TX pin an output and writing '1' to it, to not disturb the transmit line.

10. Module: EUSART

This module may perform incorrect auto-baud calculation if the ABDEN (BAUDCTL<0>) bit was set while the receive pin was at a low level.

Work around

Wait for the RX pin to go high and then set the ABDEN bit.

11. Module: EUSART

In Asynchronous Receiver mode, the EUSART does not load the SPBRGH value after completion of auto-baud.

Work around

Do not enable the BRG16 (BAUDCTL<3>) bit.

If the BRG16 is in use, ensure that the auto-baud SPBRG value does not exceed the 8-bit value.

12. Module: EUSART

The CREN (RCSTA<4>) bit is cleared after every auto-baud operation.

Work around

Upon completion of auto-baud, manually set the CREN bit.

13. Module: EUSART

Writing to the USART/EUSART TXREG register faster than the baud rate in Synchronous mode will overwrite the previous value instead of double-buffering, as in Asynchronous mode.

Work around

Load the first character into TXREG and then wait for a TX interrupt, or check the TXIF bit before writing each additional character to TXREG.

14. Module: EUSART

The EUSART cannot receive asynchronous data at the four fastest baud rates (BRGH = 1, BRG16 = 1 and SPBRG < 4).

Work around

Use a slower baud rate or a faster system clock speed.

15. Module: HSADC

A ΔI_{AD} (parameter D026) of greater than 300 µA (for V_{DD} = 3V) is observed when the device is put into Sleep mode with the HSADC enabled (ADON = 1) without setting the GO/DONE bit so that at least one conversion is performed.

Observed ΔI_{AD} will increase in proportion to V_{DD}.

Work around

If no conversion will be done while in Sleep mode, disable the HSADC module by clearing the ADON bit before entering Sleep mode.

If power consumption is an issue for the application, do not put the part into Sleep mode with the HSADC enabled if no conversion is to be performed.

REVISION HISTORY

Rev A Document (6/2004)
First revision of this document. Silicon issues 1-6 (PCPWM), 7 (Core – DAW Instruction) and 8-14 (EUSART) and Data Sheet Clarification issues 1 (Power-on Reset), 2 (Watchdog Timer), 3 (PWM Equations), 4 (DC Characteristics) and 5 (LVD Characteristics).

Rev B Document (12/2004)
Added Data Sheet Clarification issue 6 (28-Pin QFN Diagram).

Rev C Document (05/2005)
Added silicon issue 15 (HSADC). All Data Sheet Clarification issues were removed and placed into a separate Data Sheet Errata.

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