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# FIN1215 / FIN1216 / FIN1217/ FIN1218
# LVDS 21-Bit Serializers / De-Serializers

## Features

- Low Power Consumption
- 20MHz to 85MHz Shift Clock Support
- 50% Duty Cycle on the Clock Output of Receiver
- ±1V Common-mode Range ~1.2V
- Narrow Bus Reduces Cable Size and Cost
- High Throughput: 1.785Gbps
- Up to 595Mbps per Channel
- Internal PLL with No External Components
- Compatible with TIA/EIA-644 Specification
- Offered in 48-lead TSSOP Packages

## Description

The FIN1217 and FIN1215 transform 21-bit wide parallel LVTTL (Low-Voltage TTL) data into three serial LVDS (Low-Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data stream over a separate LVDS link. Every cycle of transmit clock, 21 bits of input LVTTL data are sampled and transmitted.

The FIN1216 and FIN1218 receives and converts the three serial LVDS data streams back into 21 bits of LVTTL data. Table 1 provides a matrix summary of the serializers and de-serializers available. For the FIN1217, at a transmit clock frequency of 85MHz, 21 bits of LVTTL data are transmitted at a rate of 595Mbps per LVDS channel.

These chipsets solve EMI and cable size problems associated with wide and high-speed TTL interfaces.

## Ordering Information

| Part Number | Operating Temperature Range | Eco Status | Package | Packing Method |
|---|---|---|---|---|
| FIN1215MTDX | -40 to + 85°C | RoHS | 48-Lead Thin Shrink Small Outline Package (TSSOP) | Tape and Reel |
| FIN1216MTDX | | | | |
| FIN1217MTDX | | | | |
| FIN1218MTDX (Preliminary) | | | | |

*For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.*

## Block Diagrams

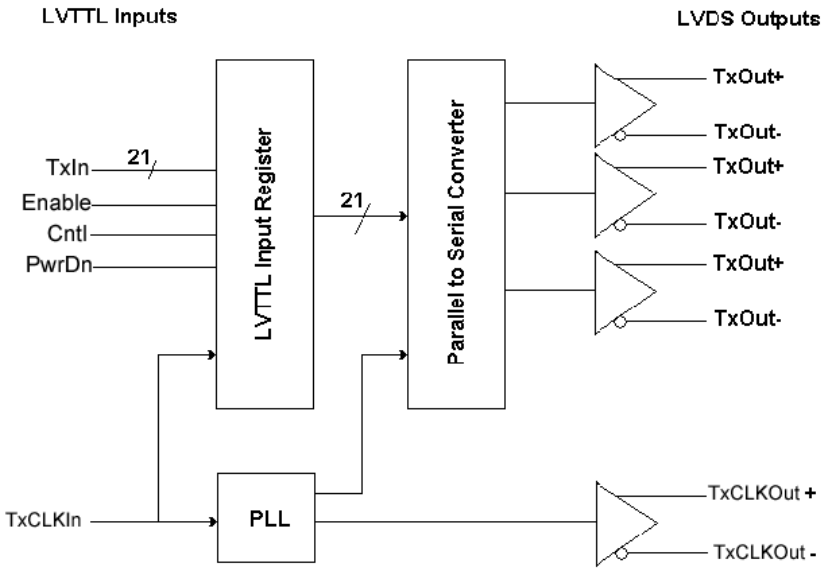


**Figure 1. FIN1217 / FIN1215 Transmitter Functional Diagram**

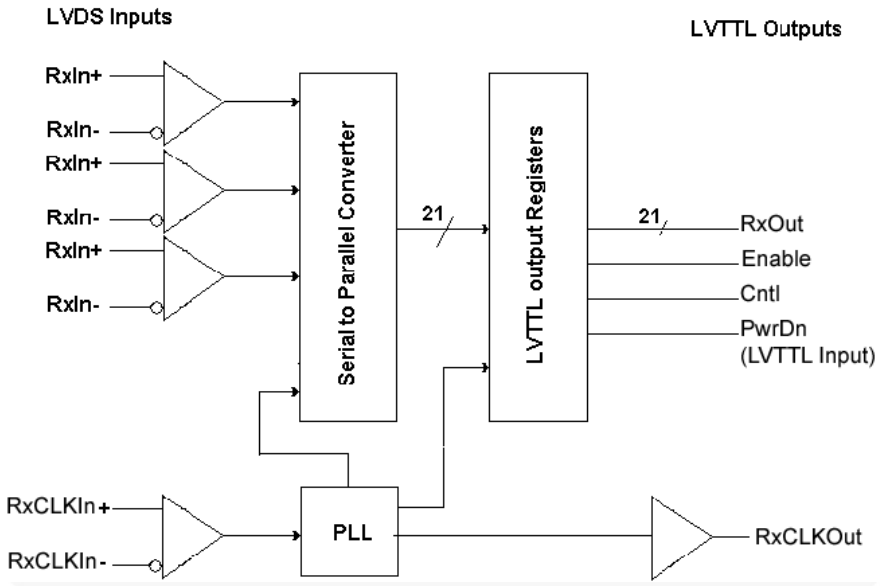


**Figure 2. FIN1218 / FIN1216 Receiver Functional Diagram**

**Table 1. Serializers / De-Serializers Chip Matrix**

| Part | CLK Frequency | LVTTL IN | LVDS OUT | LVDS IN | LVTTL OUT | Package |
|---|---|---|---|---|---|---|
| FIN1215 | 66 | 21 | 3 | | | 48-Lead TSSOP |
| FIN1216 | 66 | | | 3 | 21 | 48-Lead TSSOP |
| FIN1217 | 85 | 21 | 3 | | | 48-Lead TSSOP |
| FIN1218 | 85 | | | 3 | 21 | 48-Lead TSSOP |

## Transmitters

### Pin Configuration

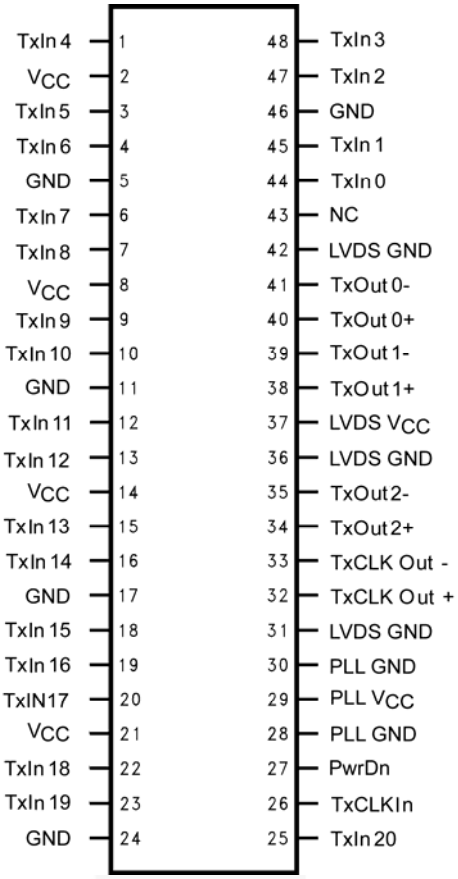


**Figure 3. FIN1217 / FIN1215 (21:3 Transmitter)**

## Pin Definitions

| Pin Names | I/O Type | # of Pins | Description of Signals |
|---|---|---|---|
| TxIn | I | 21 | LVTTL Level Inputs |
| TxCKLIn | I | 1 | LVTTL Level Clock Input; the rising edge is for data strobe |
| TxOut+ | O | 3 | Positive LVDS Differential Data Output |
| TxOut | O | 3 | Negative LVDS Differential Data Output |
| TxCLKOut+ | O | 1 | Positive LVDS Differential Clock Output |
| TxCLKOut- | O | 1 | Negative LVDS Differential Clock Output |
| /PwrDn | I | 1 | LVTTL Level Power-Down Input; assertion (LOW) puts the outputs in high-impedance state |
| PLL $V_{CC}$ | I | 1 | Power Supply Pin for LVDS Outputs |
| PLL GND | I | 2 | Ground Pins for PLL |
| LVDS $V_{CC}$ | I | 1 | Power Supply Pins for LVDS Outputs |
| LVDS GND | I | 3 | Ground Pin for LVDS Outputs |
| $V_{CC}$ | I | 4 | Power Supply Pins for LVTTL Inputs |
| GND | I | 5 | Ground Pins for LVTTL Inputs |
| NC | | | No Connect |

## Receivers

### Pin Configuration

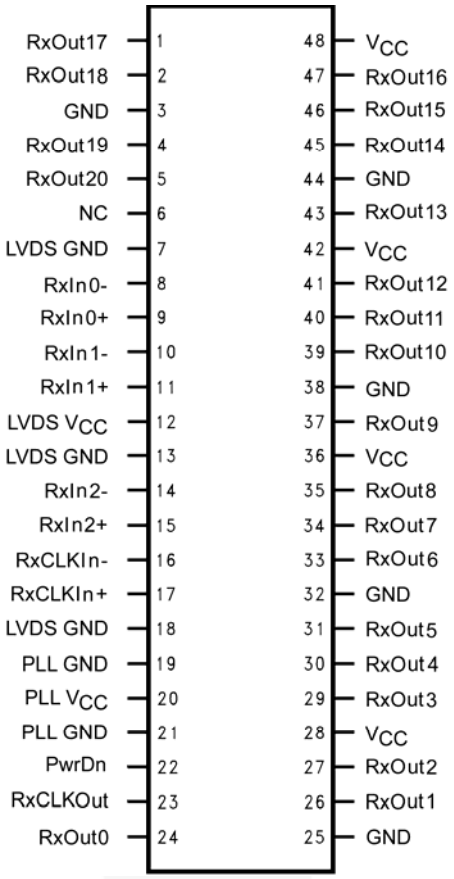


**Figure 4. FIN1216 / FIN1218 (3:21 Receiver)**

## Pin Definitions

| Pin Names | I/O Type | # of Pins | Description of Signals |
|---|---|---|---|
| RxIn | I | 3 | Negative LVDS Differential Data Output |
| RxIn+ | I | 3 | Positive LVDS Differential Data Output |
| RxCLKIn- | I | 1 | Negative LVDS Differential Clock Output |
| RxCLKIn+ | I | 1 | Positive LVDS Differential Clock Output |
| RxOut- | O | 21 | LVTTL Level Data Outputs Goes HIGH for /PwrDn LOW |
| RxCLKOut | O | 1 | LVTTL Level Clock Output |
| /PwrDn | I | 1 | LVTTL Level Input; Refer to Transmitter and Receiver Power-up and Power-down Operation Truth Table |
| PLL $V_{CC}$ | I | 1 | Power Supply Pin for PLL |
| PLL GND | I | 2 | Ground Pins for PLL |
| LVDS $V_{CC}$ | I | 1 | Power Supply Pins for LVDS Inputs |
| LVDS GND | I | 3 | Ground Pin for LVDS Inputs |
| $V_{CC}$ | I | 4 | Power Supply Pins for LVTTL Outputs |
| GND | I | 5 | Ground Pins for LVTTL Outputs |
| NC | | | No Connect |

## Truth Tables

### Transmitter

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **TxIn** | **TxCLKIn** | **PwrDn(1)** | **TxOut±** | **TxCLKOut±** |
| Active | Active | HIGH | LOW / HIGH | LOW / HIGH |
| Active | LOW / HIGH<br>High Impedance | HIGH | LOW / HIGH | Don't Care(2) |
| Floating | Active | HIGH | LOW | LOW / HIGH |
| Floating | Floating | HIGH | LOW | Don't Care(2) |
| Don't Care | Don't Care | LOW | High Impedance | High Impedance |

**Notes**:
1. The outputs of the transmitter or receiver remain in a high-impedance state until $V_{CC}$ reaches 2V.
2. TxCLKOut± settles at a free running frequency when the part is powered up, PwrDn is HIGH and the TxCLKIn is a steady logic level LOW / HIGH / high-impedance.

### Receiver

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **RxIn±** | **RxCLKIn±** | **/PwrDn(3)** | **RxOut** | **RxCLKOut** |
| Active | Active | HIGH | LOW / HIGH | LOW / HIGH |
| Active | Failsafe Condition(4) | HIGH | Last Valid State | HIGH |
| Failsafe Condition(4) | Active | HIGH | HIGH | LOW / HIGH |
| Failsafe Condition(4) | Failsafe Condition(4) | HIGH | Last Valid State(5) | HIGH |
| Don't Care | Don't Care | LOW | LOW | HIGH |

**Notes**:
3. The outputs of the transmitter or receiver remain in a high-impedance state until $V_{CC}$ reaches 2V.
4. Failsafe condition is defined as the input being terminated and un-driven, shorted, or open.
5. If RxCLKIn± is removed prior to the RxIn± date being removed, RxOut is the last valid state. If RxIn± data is removed prior to RxCLKIn± being removed, RxOut is HIGH.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | | -0.3 | +4.6 | V |
| $V_{TTL}$ | TTL/CMOS Input/Output Voltage | | -0.5 | +4.6 | V |
| $V_{LVDS}$ | LVDS Input/Output Voltage | | -0.3 | +4.6 | V |
| $I_{OSD}$ | LVDS Output Short-Circuit Current | | | Continuous | |
| $T_{STG}$ | Storage Temperature Range | | -65 | +150 | °C |
| $T_J$ | Maximum Junction Temperature, Soldering 4 seconds | | | +150 | °C |
| $T_L$ | Lead Temperature | | | +260 | °C |
| ESD | Human Body Model, JESD22-A114 (1.5kΩ, 100pF) | LVDS I/O to Ground | | 10.0 | kV |
| | | All Pins (FIN1215, FIN1217) | | 6.5 | |
| | Machine Model, JESD22-A115, 0Ω, 200pF | FIN1215, FIN1217 Only | | >400 | V |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 3.0 | 3.6 | V |
| $T_A$ | Operating Temperature | -40 | +85 | °C |
| $V_{CCNPP}$ | Maximum Supply Noise Voltage[6] | | 100 | $mV_{PP}$ |

**Note**:

6. 100mV $V_{CC}$ noise should be tested for frequency at least up to 2MHz. All the specifications should be met under such a noise level.

## Transmitter DC Electrical Characteristics

Typical values are at $T_A$=25°C and with $V_{CC}$=3.3V; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Transmitter LVTTL Input Characteristics** | | | | | | | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage | | | GND | | 0.8 | V |
| $V_{IK}$ | Input Clamp Voltage | $I_{IK}$=-18mA | | | -0.79 | -1.50 | V |
| $I_{IN}$ | Input Current | $V_{IN}$=0.4V to 4.6V | | | 1.8 | 10.0 | μA |
| | | $V_{IN}$=GND | | -10.0 | 0 | | |
| **Transmitter LVDS Output Characteristics**[7] | | | | | | | |
| $V_{OD}$ | Output Differential Voltage | $R_L$=100Ω, Figure 4 | | 250 | | 450 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change from Differential LOW-to-HIGH | | | | | 35 | mV |
| $V_{OS}$ | Offset Voltage | | | 1.125 | 1.250 | 1.375 | V |
| $\Delta V_{OS}$ | Offset Magnitude Change from Differential LOW-to-HIGH | | | | 25 | | mV |
| $I_{OS}$ | Short-Circuit Output Current | $V_{OUT}$=0V | | | -3.5 | -5.0 | mA |
| $I_{OZ}$ | Disabled Output Leakage Current | $D_O$=0V to 4.6V, /PwrDn=0V | | | ±1.0 | ±10.0 | μA |
| **Transmitter Supply Current** | | | | | | | |
| $I_{CCWT}$ | 21:3 Transmitter Power Supply Current for Worst-Case Pattern with Load[8, 9] | $R_L$=100Ω, Figure 7 | 33MHz | | 28.0 | 46.2 | mA |
| | | | 40MHz | | 29.0 | 51.7 | |
| | | | 65MHz | | 34.0 | 57.2 | |
| | | | 85MHz[10] | | 39.0 | 62.7 | |
| $I_{CCPDT}$ | Powered-Down Supply Current | /PwrDn=0.8V | | | 10.0 | 55.0 | μA |

**Notes**:

7. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltages are referenced to ground unless otherwise specified (except $\Delta V_{OD}$ and $V_{OD}$).
8. The power supply current for both transmitter and receiver can be different with the number of active I/O channels.
9. The 16-grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.
10. FIN1217 only.

## Transmitter AC Electrical Characteristics

Typical values are at over supply voltages and operating temperatures ranges, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{TCP}$ | Transmit Clock Period | Figure 10 | 11.76 | T | 50.00 | ns |
| $t_{TCH}$ | Transmit Clock (TxCLKIn) HIGH Time | | 0.35 | 0.50 | 0.65 | T |
| $t_{TCL}$ | Transmit Clock LOW Time | | 0.35 | 0.50 | 0.65 | T |
| $t_{CLKT}$ | TxCLKIn Transition Time (Rising and Falling) | 10% to 90%<br>Figure 11 | 1.0 | | 6.0 | ns |
| $t_{JIT}$ | TxCLKIn Cycle-to-Cycle Jitter | | | | 3.0 | ns |
| $t_{XIT}$ | TxIn Transition Time | | 1.5 | | 6.0 | ns |
| **LVDS Transmitter Timing Characteristics** | | | | | | |
| $t_{TLH}$ | Differential Output Rise Time (20% to 80%) | Figure 8 | | 0.75 | 1.50 | ns |
| $t_{THL}$ | Differential Output Fall Time (80% to 20%) | | | 0.75 | 1.50 | ns |
| $t_{STC}$ | TxIn Setup to TxCLNIn | Figure 10<br>f=85MHz FIN1217 only | 2.5 | | | ns |
| $t_{HTC}$ | TxIn Holds to TCLKIn | | 0 | | | ns |
| $t_{TPDD}$ | Transmitter Power-Down Delay | Figure 17[11] | | | 100 | ns |
| $t_{TCCD}$ | Transmitter Clock Input to Clock Output Delay | Figure 13<br>$T_A$=25°C, $V_{CC}$=3.3V | 2.8 | 5.5 | 6.8 | ns |
| **Transmitter Output Data Jitter** (f=40 MHz)[12] | | | | | | |
| $t_{TPPB0}$ | Transmitter Output Pulse Position of Bit 0 | Figure 20<br>$a = \frac{1}{f \times 7}$ | -0.25 | 0 | 0.25 | ns |
| $t_{TPPB1}$ | Transmitter Output Pulse Position of Bit 1 | | a-0.25 | a | a+0.25 | ns |
| $t_{TPPB2}$ | Transmitter Output Pulse Position of Bit 2 | | 2a-0.25 | 2a | 2a+0.25 | ns |
| $t_{TPPB3}$ | Transmitter Output Pulse Position of Bit 3 | | 3a-0.25 | 3a | 3a+0.25 | ns |
| $t_{TPPB4}$ | Transmitter Output Pulse Position of Bit 4 | | 4a-0.25 | 4a | 4a+0.25 | ns |
| $t_{TPPB5}$ | Transmitter Output Pulse Position of Bit 5 | | 5a-0.25 | 5a | 5a+0.25 | ns |
| $t_{TPPB6}$ | Transmitter Output Pulse Position of Bit 6 | | 6a-0.25 | 6a | 6a+0.25 | ns |
| **Transmitter Output Data Jitter** (f=65 MHz)[12] | | | | | | |
| $t_{TPPB0}$ | Transmitter Output Pulse Position of Bit 0 | Figure 20<br>$a = \frac{1}{f \times 7}$ | -0.2 | 0 | 0.2 | ns |
| $t_{TPPB1}$ | Transmitter Output Pulse Position of Bit 1 | | a-0.2 | a | a+0.2 | ns |
| $t_{TPPB2}$ | Transmitter Output Pulse Position of Bit 2 | | 2a-0.2 | 2a | 2a+0.2 | ns |
| $t_{TPPB3}$ | Transmitter Output Pulse Position of Bit 3 | | 3a-0.2 | 3a | 3a+0.2 | ns |
| $t_{TPPB4}$ | Transmitter Output Pulse Position of Bit 4 | | 4a-0.2 | 4a | 4a+0.2 | ns |
| $t_{TPPB5}$ | Transmitter Output Pulse Position of Bit 5 | | 5a-0.2 | 5a | 5a+0.2 | ns |
| $t_{TPPB6}$ | Transmitter Output Pulse Position of Bit 6 | | 6a-0.2 | 6a | 6a+0.2 | ns |

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## Transmitter AC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Transmitter Output Data Jitter** (f=85 MHz, FIN1217 only)[12] | | | | | | |
| $t_{TPPB0}$ | Transmitter Output Pulse Position of Bit 0 | Figure 20 $a = \frac{1}{f \times 7}$ | -0.2 | 0 | 0.2 | ns |
| $t_{TPPB1}$ | Transmitter Output Pulse Position of Bit 1 | | a-0.2 | a | a+0.2 | ns |
| $t_{TPPB2}$ | Transmitter Output Pulse Position of Bit 2 | | 2a-0.2 | 2a | 2a+0.2 | ns |
| $t_{TPPB3}$ | Transmitter Output Pulse Position of Bit 3 | | 3a-0.2 | 3a | 3a+0.2 | ns |
| $t_{TPPB4}$ | Transmitter Output Pulse Position of Bit 4 | | 4a-0.2 | 4a | 4a+0.2 | ns |
| $t_{TPPB5}$ | Transmitter Output Pulse Position of Bit 5 | | 5a-0.2 | 5a | 5a+0.2 | ns |
| $t_{TPPB6}$ | Transmitter Output Pulse Position of Bit 6 | | 6a-0.2 | 6a | 6a+0.2 | ns |
| $t_{JCC}$ | Transmitter Clock Out Jitter, Cycle-to cycle Figure 23 | f=40MHz | | 350 | 370 | ps |
| | | f=65MHz | | 210 | 230 | |
| | | f=85MHz FIN1217 only | | 110 | 150 | |
| $t_{TPLLS}$ | Transmitter Phase Lock Loop Set Time[13] | Figure 15[12] | | | 10.0 | ms |

**Notes**:

11. Outputs of all transmitters stay in 3-STATE until power reaches 2V. Clock and data output begins to toggle 10ms after $V_{CC}$ reaches 3V and /PwrDn pin is above 1.5V.
12. This output data pulse position works for both transmitters with 21 TTL inputs, except the LVDS output bit mapping difference (see Figure 19). Figure 20 shows the skew between the first data bit and clock output. A two-bit cycle delay is guaranteed when the MSB is output from transmitter.
13. This jitter specification is based on the assumption that PLL has a reference clock with cycle-to-cycle input jitter of less than 2ns.

## Receiver DC Electrical Characteristics

Typical values are at $T_A$=25°C and with $V_{CC}$=3.3V. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltages are referenced to ground unless otherwise specified (except $\Delta V_{OD}$ and $V_{OD}$). Minimum and maximum values are at over supply voltage and operating temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **LVTTL/CMOS DC Characteristics** | | | | | | | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage | | | GND | | 0.8 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$=-0.4mA | | 2.7 | 3.3 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$=2mA | | | | 0.3 | V |
| $V_{IK}$ | Input Clamp Voltage | $I_{IK}$=-18mA | | | | -1.5 | V |
| $I_{IN}$ | Input Current | $V_{IN}$=0V to 4.6V | | -10 | | 10 | µA |
| $I_{OFF}$ | Input/Output Power-Off Leakage Current | $V_{CC}$=0V, All LVTTL Inputs/Outputs 0V to 4.6V | | | | ±10 | µA |
| $I_{OS}$ | Output Short-Circuit Current | $V_{OUT}$=0V | | | -60 | -120 | µA |
| **Receiver LVDS Input Characteristics** | | | | | | | |
| $V_{TH}$ | Differential Input Threshold HIGH | Figure 6, Table 2 | | | | 100 | mV |
| $V_{TL}$ | Differential Input Threshold LOW | Figure 6, Table 2 | | -100 | | | mV |
| $V_{ICM}$ | Input Common Mode Range | Figure 6, Table 2 | | 0.05 | | 2.35 | V |
| $I_{IN}$ | Input Current | $V_{IN}$=2.4V, $V_{CC}$=3.6V or 0V | | | | ±10.0 | µA |
| | | $V_{IN}$=0V, $V_{CC}$=3.6V or 0V | | | | ±10.0 | |
| **Receiver Supply Current** | | | | | | | |
| $I_{CCWR}$ | 3:21 Receiver Power Supply Current for Worst Case Pattern with Load[14] | $C_L$=8pF, Figure 7 | 33MHz | | | 66 | mA |
| | | | 40MHz | | 56 | 74 | |
| | | | 65MHz | | 75 | 102 | |
| | | | 85MHz[15] | | 92 | 125 | |
| $I_{CCPDR}$ | Powered Down Supply Current | /PwrDn=0.8V (RxOut stays LOW) | | | NA | 400 | µA |

**Notes**:

14. The power supply current for the receiver can be different due to the number of active I/O channels.
15. 85MHz specification for FIN1218 only.

## Receiver AC Electrical Characteristics

Values are at over supply voltages and operating temperatures, unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{RCOL}$ | RxCLKOut LOW Time | Figure 12 Rising Edge Strobe f=40MHz | 10.0 | 11.0 | | ns |
| $t_{RCOH}$ | RxCLKOut HIGH Time | | 10.0 | 12.2 | | ns |
| $t_{RSRC}$ | RxOut Valid Prior to RxCLKOut | | 6.5 | 11.6 | | ns |
| $t_{RHRC}$ | RxOut Valid After RxCLKOut | | 6.0 | 11.6 | | ns |
| $t_{RCOP}$ | Receiver Clock Output (RxCLKOut) Period | Figure 12 Rising Edge Strobe f=65MHz | 15.0 | T | 50.0 | ns |
| $t_{RCOL}$ | RxCLKOut LOW Time | | 5.0 | 7.8 | 9.0 | ns |
| $t_{RCOH}$ | RxCLKOut HIGH Time | | 5.0 | 7.3 | 9.0 | ns |
| $t_{RSRC}$ | RxOut Valid Prior to RxCLKOut | | 4.5 | 7.7 | | ns |
| $t_{RHRC}$ | RxOut Valid After RxCLKOut | | 4.0 | 8.4 | | ns |
| $t_{RCOP}$ | Receiver Clock Output (RxCLKOut) Period | Figure 12 Rising Edge Strobe f=85MHz FIN1218 only | 11.76 | T | 50.00 | ns |
| $t_{RCOL}$ | RxCLKOut LOW Time | | 4.0 | 6.3 | 6.0 | ns |
| $t_{RCOH}$ | RxCLKOut HIGH Time | | 4.5 | 5.4 | 6.5 | ns |
| $t_{RSRC}$ | RxOut Valid Prior to RxCLKOut | | 3.5 | 6.3 | | ns |
| $t_{RHRC}$ | RxOut Valid After RxCLKOut | | 3.5 | 6.5 | | ns |
| $t_{ROLH}$ | Output Rise Time (20% to 80%) | $C_L$=8pF, Figure 9 | | 2.2 | 5.0 | ns |
| $t_{ROHL}$ | Output Fall Time (80% to 20%) | | | 2.1 | 5.0 | ns |
| $t_{RCCD}$ | Receiver Clock Input to Clock Output Delay | $T_A$=25°C, $V_{CC}$=3.3V Figure 14 (**Error! Reference source not found.**) | 3.5 | 6.9 | 7.5 | ns |
| $t_{RPDD}$ | Receiver Power-Down Delay | Figure 18 | | | 1.0 | ms |
| $t_{RSPB0}$ | Receiver Input Strobe Position of Bit 0 | Figure 21 f=40MHz | 1.00 | | 2.15 | ns |
| $t_{RSPB1}$ | Receiver Input Strobe Position of Bit 1 | | 4.5 | | 5.8 | ns |
| $t_{RSPB2}$ | Receiver Input Strobe Position of Bit 2 | | 8.10 | | 9.15 | ns |
| $t_{RSPB3}$ | Receiver Input Strobe Position of Bit 3 | | 11.6 | | 12.6 | ns |
| $t_{RSPB4}$ | Receiver Input Strobe Position of Bit 4 | | 15.1 | | 16.3 | ns |
| $t_{RSPB5}$ | Receiver Input Strobe Position of Bit 5 | | 18.8 | | 19.9 | ns |
| $t_{RSPB6}$ | Receiver Input Strobe Position of Bit 6 | | 22.5 | | 23.6 | ns |

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## Receiver AC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{RSPB0}$ | Receiver Input Strobe Position of Bit 0 | Figure 21 f=65MHz | 0.7 | | 1.4 | ns |
| $t_{RSPB1}$ | Receiver Input Strobe Position of Bit 1 | | 2.9 | | 3.6 | ns |
| $t_{RSPB2}$ | Receiver Input Strobe Position of Bit 2 | | 5.1 | | 5.8 | ns |
| $t_{RSPB3}$ | Receiver Input Strobe Position of Bit 3 | | 7.3 | | 8.0 | ns |
| $t_{RSPB4}$ | Receiver Input Strobe Position of Bit 4 | | 9.5 | | 10.2 | ns |
| $t_{RSPB5}$ | Receiver Input Strobe Position of Bit 5 | | 11.7 | | 12.4 | ns |
| $t_{RSPB6}$ | Receiver Input Strobe Position of Bit 6 | | 13.9 | | 14.6 | ns |
| $t_{RSPB0}$ | Receiver Input Strobe Position of Bit 0 | Figure 21 f=85MHz FIN1218 only | 0.49 | | 1.19 | ns |
| $t_{RSPB1}$ | Receiver Input Strobe Position of Bit 1 | | 2.17 | | 2.87 | ns |
| $t_{RSPB2}$ | Receiver Input Strobe Position of Bit 2 | | 3.85 | | 4.55 | ns |
| $t_{RSPB3}$ | Receiver Input Strobe Position of Bit 3 | | 5.53 | | 6.23 | ns |
| $t_{RSPB4}$ | Receiver Input Strobe Position of Bit 4 | | 7.21 | | 7.91 | ns |
| $t_{RSPB5}$ | Receiver Input Strobe Position of Bit 5 | | 8.89 | | 9.59 | ns |
| $t_{RSPB6}$ | Receiver Input Strobe Position of Bit 6 | | 10.57 | | 11.27 | ns |
| $t_{RSKM}$ | RxIn Skew Margin[**Error! Reference source not found.**] | f=40MHz, Figure 22 | 490 | | | ps |
| | | f=65MHz, Figure 22 | 400 | | | |
| | | f=85MHz FIN1218 only Figure 22 | 252 | | | |
| $t_{RPLLS}$ | Receiver Phase Lock Loop Set Time | Figure 16 | | | 10.0 | ms |

**Notes:**

16. Total channel latency from serializer to deserializer is $(T + t_{TCCD}) + (2 \bullet T + t_{RCCD})$.
17. Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum/maximum bit position.

## Test Circuits

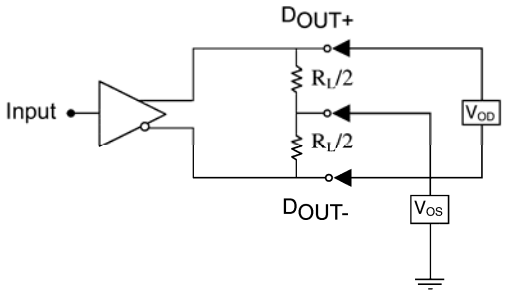
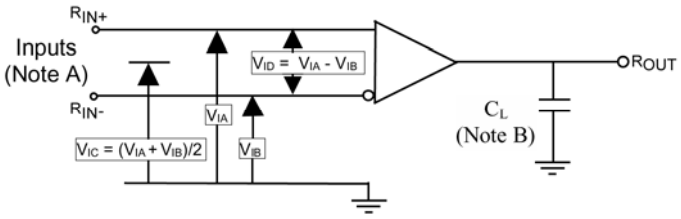



**Figure 5. Differential LVDS Output DC Test Circuit**



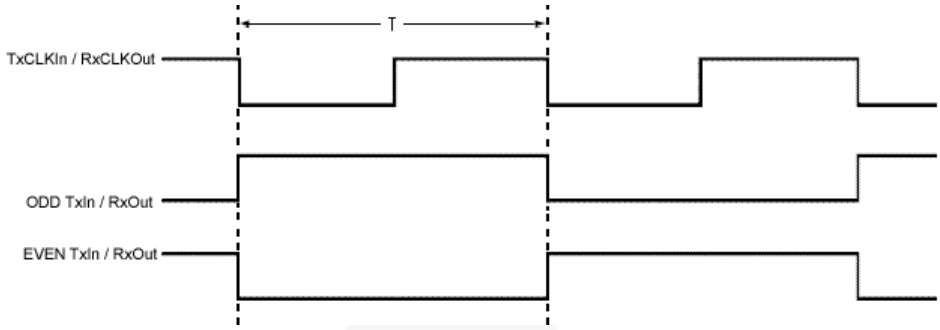

Notes: For all input pulses, $t_R$ or $t_F$<=1ns.
$C_L$ includes all probe and jig capacitance.

**Figure 6. Differential Receiver Voltage Definitions, Propagation Delay, and Transition Time Test Circuit**

**Table 2. Receiver Minimum and Maximum Input Threshold Test Voltages**

| Applied Voltages (V) | | Resulting Differential Input Voltage (mV) | Resulting Common Mode Input Voltage (V) |
|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ |
| 1.25 | 1.15 | 100 | 1.20 |
| 1.15 | 1.25 | -100 | 1.20 |
| 2.40 | 2.30 | 100 | 2.35 |
| 2.30 | 2.40 | -100 | 2.35 |
| 0.10 | 0 | 100 | 0.05 |
| 0 | 0.10 | -100 | 0.05 |
| 1.50 | 0.90 | 600 | 1.20 |
| 0.90 | 1.50 | -600 | 1.20 |
| 2.40 | 1.80 | 600 | 2.10 |
| 1.80 | 2.40 | -600 | 2.10 |
| 0.60 | 0 | 600 | 0.30 |
| 0 | 0.60 | -600 | 0.30 |

## AC Loadings and Waveforms




Note: The worst-case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVTTL/CMOS I/O. Depending on the valid strobe edge of transmitter, the TxCLKIn can be either rising or failing edge data strobe.

**Figure 7. Worst-Case Test Pattern**

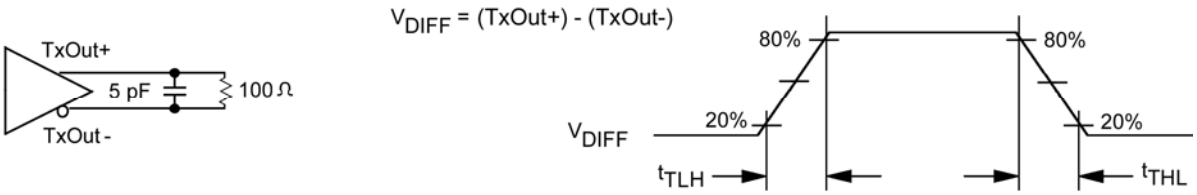



**Figure 8. Transmitter LVDS Output Load and Transition Times**

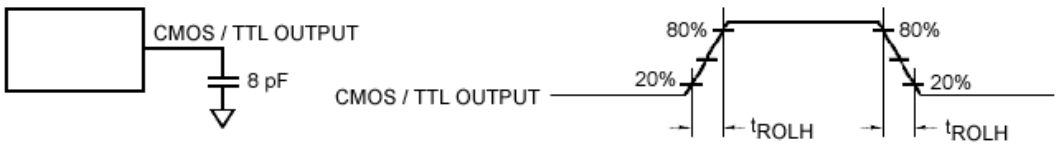



**Figure 9. Receiver LVTTL/CMOS Output Load and Transition Times**

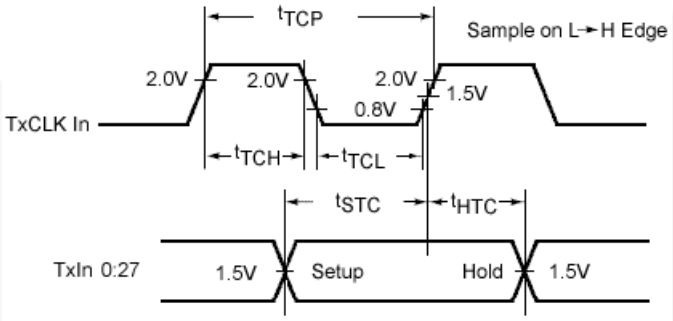



**Figure 10. Transmitter Set-up/Hold and HIGH/LOW Times (Rising Edge Strobe)**

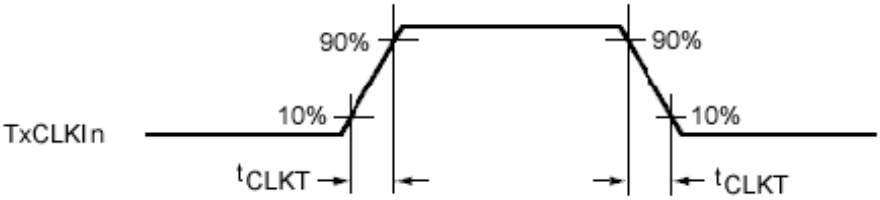



**Figure 11. Transmitter Input Clock Transition Time**

## AC Loadings and Waveforms (Continued)

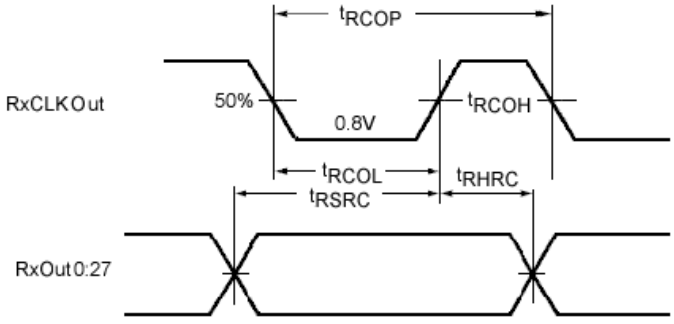



**Figure 12. Receiver Set-up/Hold and HIGH/LOW Times**

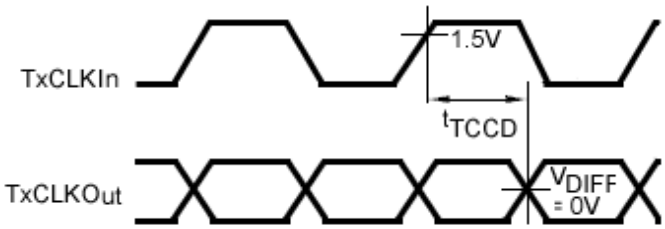



**Figure 13. Transmitter Clock-In to Clock-Out Delay (Rising Edge Strobe)**

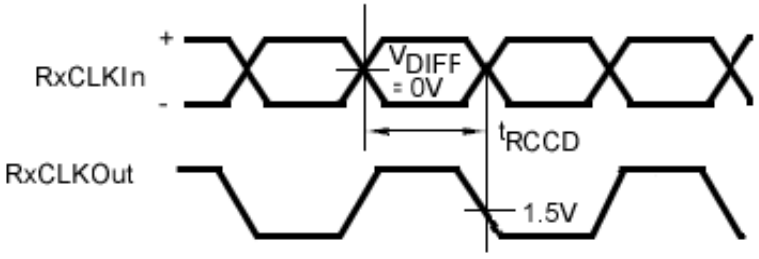



**Figure 14. Receiver Clock-In to Clock-Out Delay (Rising Edge Strobe)**

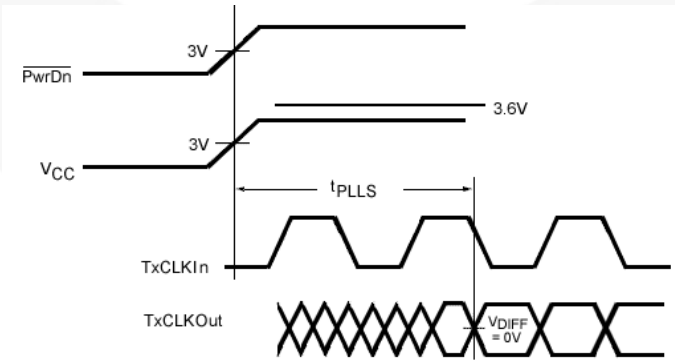



**Figure 15. Transmitter Phase-Lock-Loop Set Time**

## AC Loadings and Waveforms (Continued)

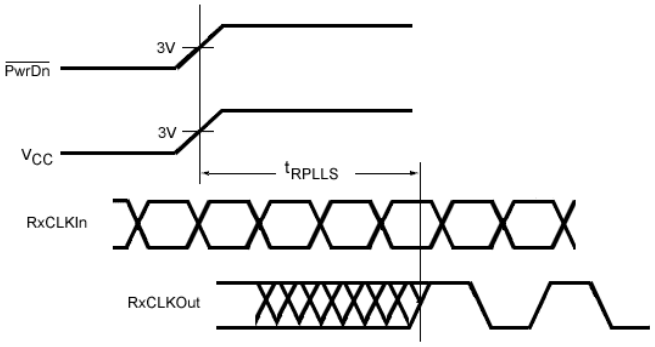



**Figure 16. Receiver Phase Lock Loop Set Time**

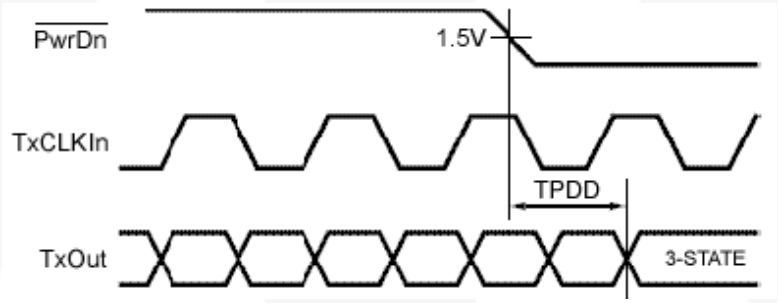



**Figure 17. Transmitter Power-down Delay**

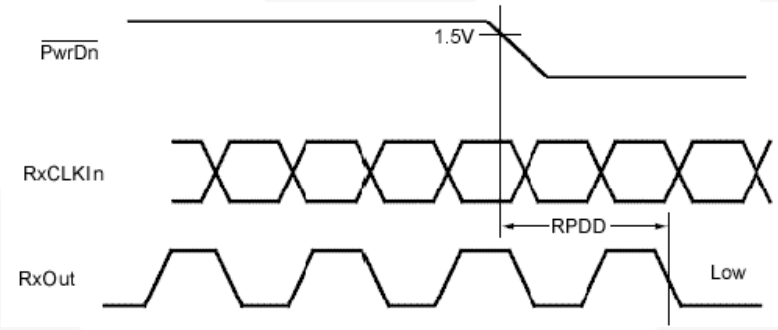
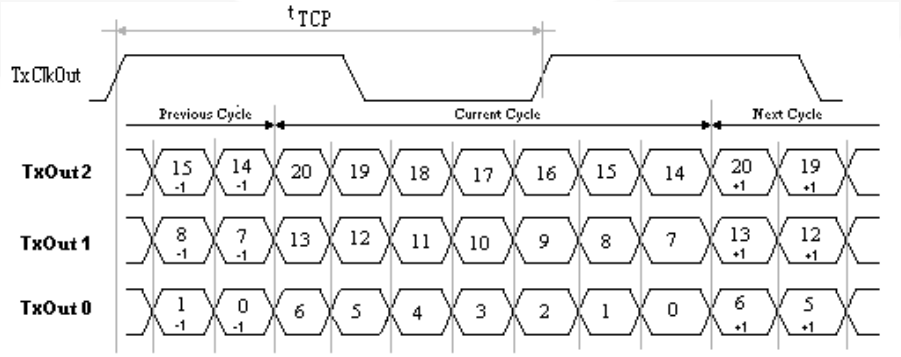



**Figure 18. Receiver Power-down Delay**




Note: This output date pulse position works for both transmitters with 21 TTL inputs, except the LVDS output bit mapping difference. Two-bit cycle delay is guaranteed with the MSB is output from transmitter.

**Figure 19. Parallel LVTTL Inputs Mapped to Three Serial LVDS Outputs**

## AC Loadings and Waveforms (Continued)]

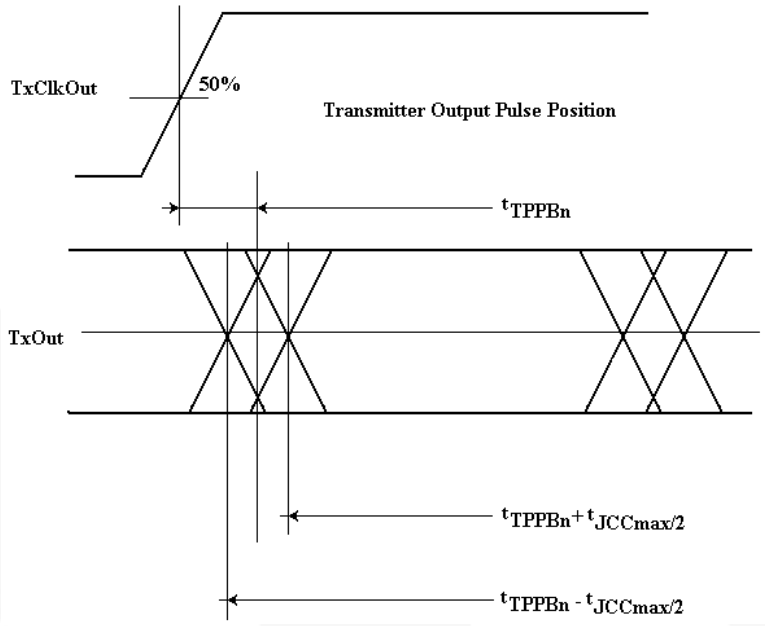



**Figure 20. Transmitter Output Pulse Bit Position**

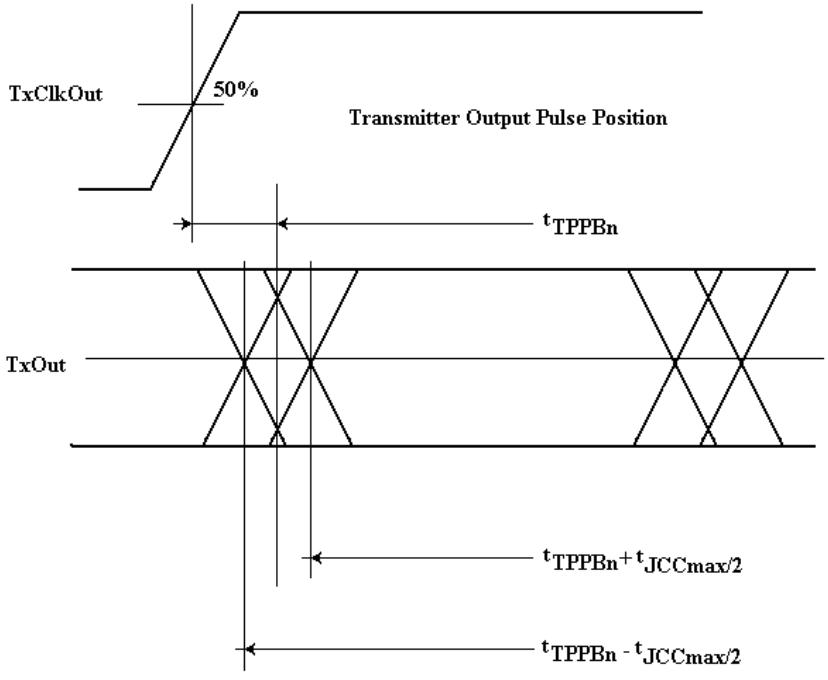
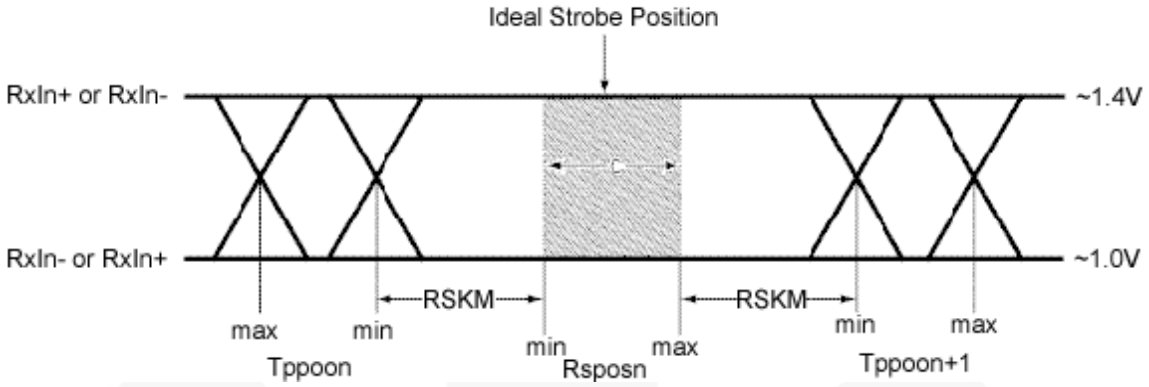


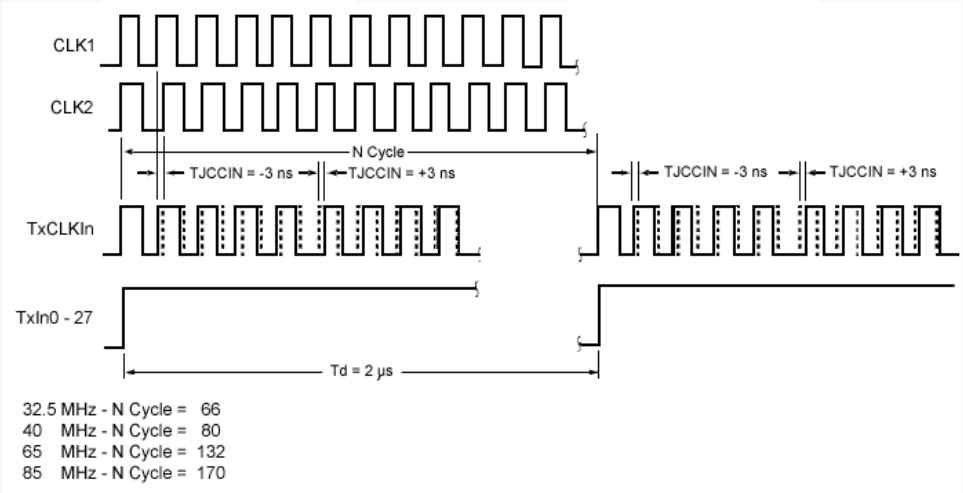

**Figure 21. Receiver Strobe Bit Position**

## AC Loadings and Waveforms (Continued)




Note: $t_{RSKM}$ is the budget for the cable skew and source clock skew plus Inter-Symbol Interference (ISI). The minimum and maximum pulse position values are based on the bit position of each of the seven bits within the LVDS data stream across PVT (Process, Voltage Supply, and Temperature).

**Figure 22. Receiver LVDS Input Skew Margin**




Note: This jitter pattern is used to test the jitter response (clock out) of the device over the power supply range with worst jitter ±ns (cycle-to-cycle) clock input. The specific test methodology is as follows:

- Switching input data TxIn0 to TxIn20 at 0.5MHz and the input clock is shifted to left -3ns and to the right +3ns when data is HIGH (by switching between CLK1 and CLK2 in Figure 11).
- The ±3ns cycle-to-cycle input jitter is the static phase error between the two clock sources. Jumping between two clock sources to simulate the worst-case of clock edge jump (3ns) from graphical controllers. Cycle-to-cycle jitter at TxCLK out pin should be measured cross $V_{CC}$ range with 100mV noise ($V_{CC}$ noise frequency <2MHz).

**Figure 23. Jitter Pattern**

## Physical Dimensions

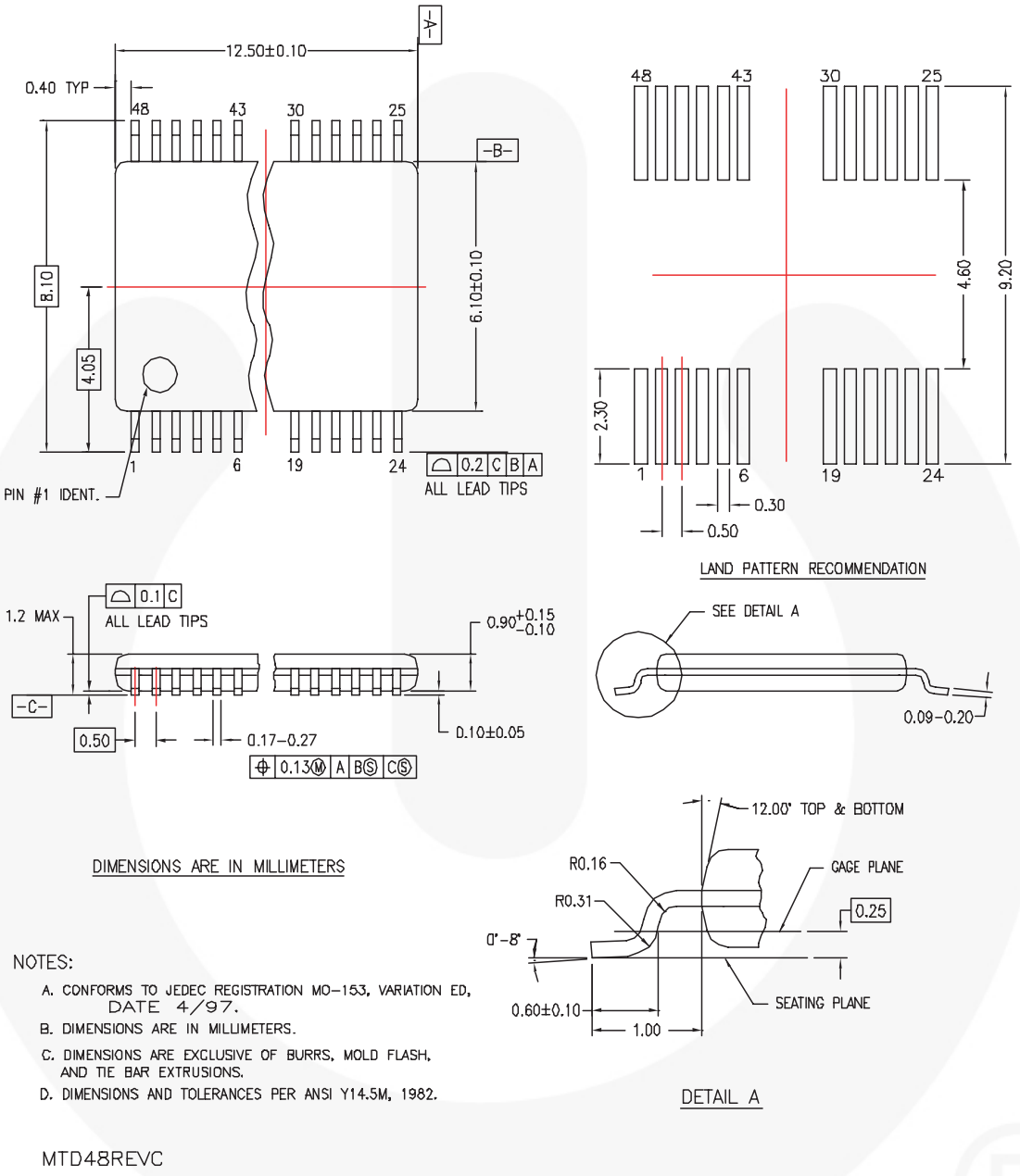



**Figure 24. 48-Lead Thin Shrink Small Outline Package (TSSOP)**

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